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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,806	06/28/2005	Simon Tam	124280	5681

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EXAMINER	
RAINEY, ROBERT R	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/538,806	TAM, SIMON	
	Examiner	Art Unit	
	ROBERT R. RAINEY	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/11/2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/13/05,9/11/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1, 3, 4, 10, and 11** rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,933,189 to *Nomura* ("*Nomura*").

As to **claim 1**, Nomura discloses a differential circuit comprising a single transistor (see for example Fig. 8 "QD") current mirror, including a capacitor (see for example Fig. 8 "CD") connected to the transistor by a switch (see for example Fig. 8 "QS"), and two current sources connected to the current mirror by respective and independent switches (see for example Fig. 8 "QT" and "QP"), the switch of one of the current sources being operated together with the capacitor switch so as to charge the capacitor and the switch of the other current source being operated so that the circuit operates as a source-follower amplifier with a current-source load (see for example Fig. 5 for switch timing information; Note that the discussion of the operation of the elements using Fig. 5 is made with respect to Fig. 3 and 4 and common elements in later embodiments are referenced back to the original description. Nomura seems to have made an inadvertent change of QS polarity between Fig. 4 and Fig. 8 so Fig. 4 must be

referenced in order to see the operation of the two modes with QS and QP on to charge the capacitor then QT on to perform the current comparison.).

As to **claim 3**, *Nomura* further discloses that one or more of the current sources is implemented as an independent transistor (transistor QA is an independent, i.e. individual transistor, it seems as independent as any other transistor).

As to **claim 4**, *Nomura* further discloses that the current sources are implemented by a single transistor with the gate thereof connected via the two said current source switches to respective voltage inputs (see for example Fig. 8).

As to **claim 10**, *Nomura* further discloses the current source connectable so that the circuit operates as a source-follower amplifier with a current-source load is the output of a sensor pixel of an active matrix sensor array (see for example Fig. 6 and 21:49-59).

As to **claim 11**, *Nomura* further discloses an electronic device having a differential circuit as claimed in claim 1 (see for example Abstract; also any instantiation of the circuit disclosed would necessarily be electronic and would thus comprise an electronic device).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 2, and 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. U.S. Patent No. 5,933,189 to *Nomura* ("*Nomura*").

As to **claim 2**, *Nomura* discloses the claimed invention except for the said switches being each implemented as an n-channel transistor. n-channel transistors were well known in the art as substitutes for p-channel transistors as disclosed by Nomura as were the tradeoffs and modifications required in order to make such substitutions. It would have been obvious to one of ordinary skill in the art at the time of the invention to substitute n-channel transistors for the p-channel transistors shown in *Nomura* and the results would have been predictable.

As to **claim 5**, in addition to the rejection of claim 4 over *Nomura*: *Nomura* discloses the claimed invention except for at least one additional switch being connected to the gate of the said current source single transistor, the additional switch being operated by a drive signal which is independent of and non-overlapping with drive signals applied to the said current source switches and

which operably applies an independent voltage to the gate of the said current source single transistor.

Multiplexers, i.e. multiple switches, each being operated by a drive signal which is independent of and non-overlapping with drive signals applied to the other switches and each operably applying an independent voltage to a detection element, were well known to those skilled in the art at the time of the invention.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to duplicate the PD-QT pair and/or QP/alternative-VP pairs and provide signals appropriate to multiplex any desired number of independent voltages into the detection node, i.e. the gate of QA. The suggestion/motivation would have been to provide advantages such as to reduce the required number of detection circuits.

As to **claim 6**, in addition to the rejection of claim 4 over *Nomura*: *Nomura* discloses the claimed invention except for the output of the current mirror is connected to a MOS input amplifier.

MOS input amplifiers were well known as was the connection of current mirrors to their inputs. Such a connection would have required no more than ordinary skill.

As to **claim 7**, in addition to the rejection of claim 4 over *Nomura*: *Nomura* discloses the claimed invention except for the output of the current mirror is connected to the input of a second single transistor current mirror.

Nomura already taught the connection of a voltage source to the input of the current mirror. It would have required no more than ordinary skill to duplicate the current mirror circuitry and use it to generate the voltage input to another single transistor current mirror.

As to **claim 8**, in addition to the rejection of claim 1 over *Nomura*: *Nomura* discloses the claimed invention except for the said two current source switches being connected to the single transistor current mirror via a transistor pair comprising two transistors connected in parallel with each other and having their gates each effectively connected with a respective one of the said two current source switches, so as to receive the respective drive signal applied to the said two current source switches.

The use of switches to connect a power source to its load only when the load is active was known in the art, for example to save power. It was also known to utilize existing signals to drive switches to implement the connect/disconnect function. Connecting switches in parallel to implement an OR function was also known. It would have been obvious to one of ordinary skill in the art at the time of the invention to connect the single transistor current source to its load only when the load was active by said two current source switches being connected to the

single transistor current mirror via a transistor pair comprising two transistors connected in parallel with each other and having their gates each effectively connected with a respective one of the said two current source switches, so as to receive the respective drive signal applied to the said two current source switches.

The suggestion/motivation would have been to provide advantages such as to save power.

As to **claim 9**, in addition to the rejection of claim 1 over *Nomura*: *Nomura* discloses the claimed invention except for the output of the said single transistor current mirror being connected to a self bias comparator via the said transistor pair.

Self bias comparators were well known as was the connection of current mirrors to their inputs. Such a connection would have required no more than ordinary skill.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT R. RAINEY whose telephone number is (571)270-3313. The examiner can normally be reached on Monday through Friday 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RR/

/Amare Mengistu/
Supervisory Patent Examiner, Art Unit 2629